

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE APPLICATION OF:

**WILLIAM J. BORLAND**

CASE NO.: **EL0509 US NA**

APPLICATION NO.:

CONFIRMATION NO.:

GROUP ART UNIT:

EXAMINER:

FILED: **HEREWITH**

**FOR: METHOD OF MAKING INNERLAYER PANELS AND PRINTED WIRING  
BOARDS USING X-RAY IDENTIFICATION OF FIDUCIALS**

**INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

In compliance with 37 CFR 1.97 and 1.98, Applicants bring to the attention of the U.S. Patent and Trademark Office information listed on the enclosed PTO/SB/08. A copy of the information is also enclosed.

Should any fee be required in connection with the filing of this Information Disclosure Statement, please charge such fee to Deposit Account No. 04-1928 (E. I. du Pont de Nemours and Company).

Respectfully submitted,



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Dated: 11/19/2003

Enclosures

Substitute for form 1449/PTO

***(Use as many sheets as necessary)***

Sheet	1	of	2
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## Application Number

Filing Date

November 11, 2003

First Named Inventor

**William J. Borland**

**Art Unit**

**Examiner Name**

Attorney Docket Number

EL 0509 US NA
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**Examiner  
Signature**

Date  
Considered

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# INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(Use as many sheets as necessary)

## Complete If Known

Application Number

Filing Date

November 11, 2003

First Named Inventor

William J. Borland

Art Unit

Examiner Name

Attorney Docket Number

EL 0509 US NA

Sheet

2

of

2

## NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T <sup>2</sup>
		FELTEN, J., FERGUSON, S., Embedded Ceramic Resistors and Capacitors in PWB - Process and Design, IPC Printed Circuits Expo, Long Beach, California, March 2002	<input type="checkbox"/>
		FELTEN, J., SNOGREN, R., AND ZHOU, J., Embedded Ceramic Resistors and Capacitors in PWB: Process and Performance, Fall IPC Meeting, Orlando, Florida, October 11, 2001	<input type="checkbox"/>
		BORLAND, W., FELTEN, J., Thick Film Ceramic Capacitors and Resistors inside Printed Circuit Boards, 34th International Symposium on Microelectronics (IMAPS), Baltimore, MD., October 9-11, 2001	<input type="checkbox"/>
			<input type="checkbox"/>
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